The nitride semiconductor device according to the present embodiment has a configuration obtained from the nitride semiconductor device according to the first embodiment shown in FIG. **1** by replacing the carrier transit layer **1** with the buffer layer **41**, the first underlying layer **42**, the second underlying layer **43** and the channel layer **44** in the nitride semiconductor device according to the fourth embodiment shown in FIG. **19**. Viewing from the nitride semiconductor device according to the fourth embodiment shown in FIG. **19**, the nitride semiconductor device according to the present embodiment has a configuration obtained by replacing the barrier layer **45** with a laminated film composed of the barrier layer **2**, the threshold control layer **3** and the carrier induction layer **4** in the nitride semiconductor device according to the first embodiment shown in FIG. **1**.

[**0119**] Owing to such a configuration, the nitride semiconductor device according to the present embodiment can have both advantages of the first embodiment and the fourth embodiment. In other words, a nitride semiconductor device in which the threshold voltage can be controlled easily and the on-resistance is low can be provided with a high yield. In addition, a normally-off type nitride semiconductor device having low on-resistance can be provided with a high yield.

[**0120**] By the way, the nitride semiconductor layer according to the present embodiment can be combined with the first to third modifications of the first embodiment, the second embodiment, the third embodiment and its modification, or the first and second modifications of the fourth embodiment. Moreover, a nitride semiconductor device having favorable pinch-off characteristics can be provided.

[**0121**] According to the embodiments of the present invention, a nitride semiconductor device in which the threshold voltage can be controlled easily and the on-resistance is low can be provided with a high yield. Furthermore, according to an embodiment of the present invention, a nitride semiconductor device having favorable pinch-off characteristics can be provided.

[**0122**] Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concepts as defined by the appended claims and their equivalents.

What is claimed is:

1. A nitride semiconductor device comprising:

a first nitride semiconductor layer formed of non-doped $Al_xGa_{1-x}N$ ($0 \leqq x < 1$);

a second nitride semiconductor layer formed on the first nitride semiconductor layer of non-doped or n-type $Al_YGa_{1-Y}N$($0 < Y \leqq 1$, $X < Y$), and having a smaller lattice constant than that of the first nitride semiconductor layer;

a third nitride semiconductor layer formed on the second nitride semiconductor layer of a non-doped or n-type nitride semiconductor, and having a lattice constant equal to that of the first nitride semiconductor layer;

a fourth nitride semiconductor layer formed on the third nitride semiconductor layer of $In_WAl_ZGa_{1-W-Z}N$ ($0 < W \leqq 1$, $0 < Z < 1$);

a gate electrode formed in a recess structure having a bottom face which arrives at the third nitride semiconductor layer; and

a source electrode and a drain electrode formed on the second nitride semiconductor layer, the third nitride semiconductor layer, or the fourth nitride semiconductor layer so as to sandwich the gate electrode therebetween.

2. The device according to claim 1, wherein the second nitride semiconductor layer has a film thickness T_2 satisfying a following inequality

$T_2 \leqq 16.4 \times (1-1.27 \times (Y-X))/(Y-X)$[Å] where (Y−X) is less than 1/1.27.

3. The device according to claim 1, further comprising:

an insulation film formed so as to cover the gate electrode, the source electrode and the drain electrode; and

a field plate electrode connected to the gate electrode or the source electrode, at least one end of the field plate electrode being located on the insulation film between an end of the gate electrode on the drain electrode side and the drain electrode.

4. The device according to claim 1, wherein the fourth nitride semiconductor layer has a film thickness in the range of 1 nm to 10 nm.

5. A nitride semiconductor device comprising:

a first nitride semiconductor layer formed of GaN;

a second nitride semiconductor layer formed on the first nitride semiconductor layer of $(In_TAl_{1-T})_SGa_{1-S}N$ ($0 < S \leqq 1$, $0 < T \leqq 1$);

a third nitride semiconductor layer formed on the second nitride semiconductor layer of $(In_YAl_{1-Y})_XGa_{1-X}N$ ($0 < X \leqq 1$, $0 \leqq Y < 1$), an In composition ratio Y of the third nitride semiconductor layer being less than an In composition ratio T of the second nitride semiconductor layer;

a fourth nitride semiconductor layer formed on the third nitride semiconductor layer of GaN or In_pGa_QN ($0 < P < 1$, $0 < Q < 1$);

a fifth nitride semiconductor layer formed on the fourth nitride semiconductor layer of $In_UAl_WGa_VN$ ($0 \leqq U < 1$, $0 \leqq V < 1$, $0 < W \leqq 1$, $U+V+W=1$);

a gate electrode formed on the fifth nitride semiconductor layer; and

a source electrode and a drain electrode formed on the fifth nitride semiconductor layer on both sides of the gate electrode.

6. The device according to claim 5, wherein the In composition ratio T of the second nitride semiconductor layer is at least 0.3 and the In composition ratio Y of the third nitride semiconductor layer is 0.3 or less.

7. The device according to claim 5, wherein the third nitride semiconductor layer has a band gap smaller than that of the second nitride semiconductor layer.